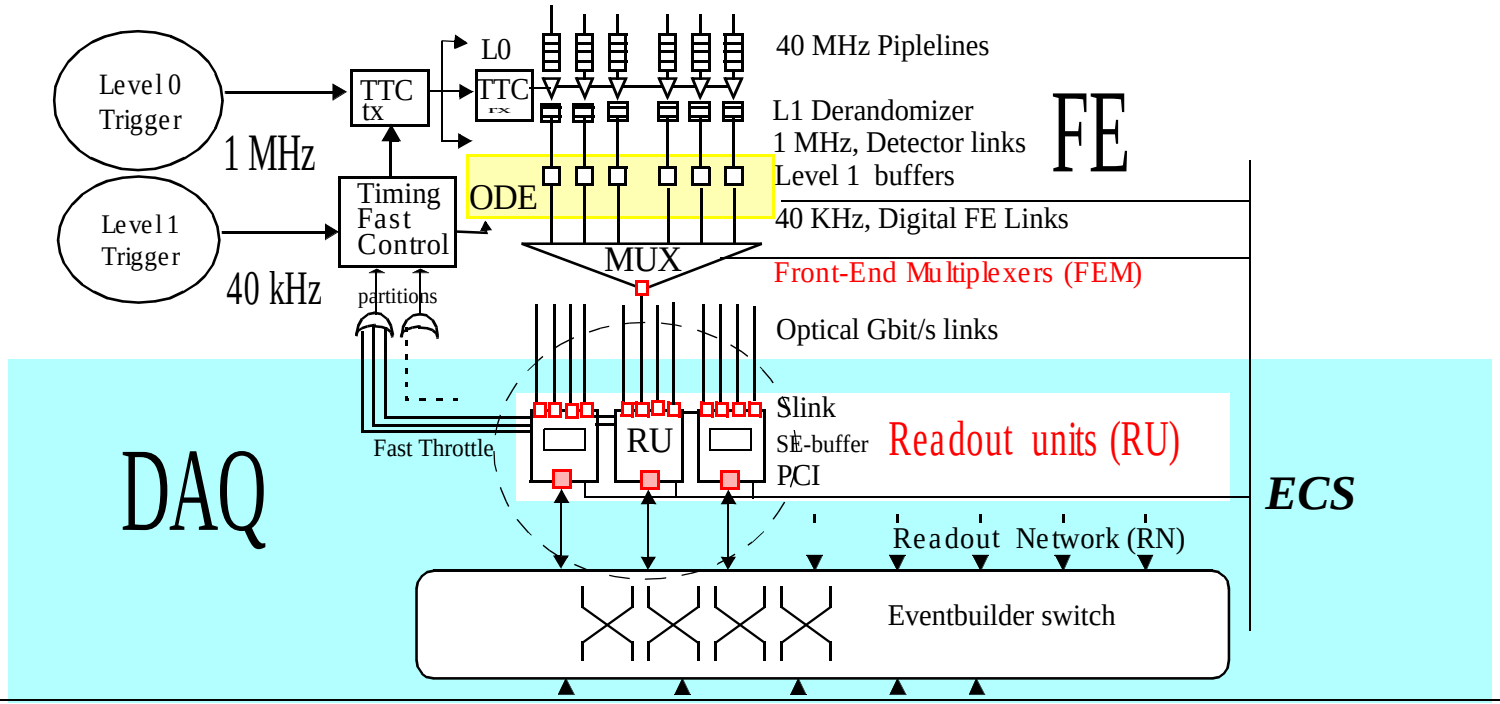
Readout Unit

Some RU topics of LHCb Mai WS '2000...

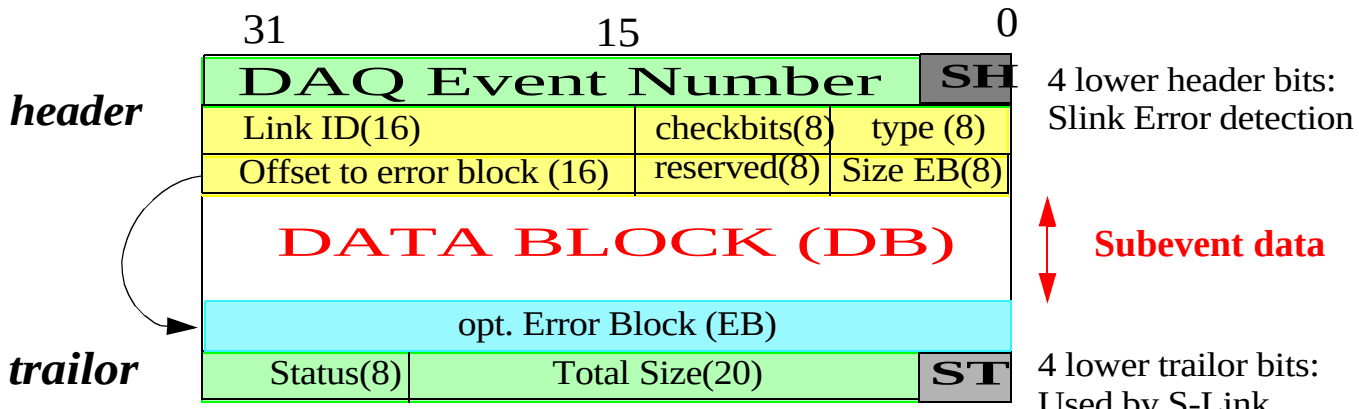


RU ' 2000

Topics:

- Data Transport Formats, Multiplexer, Input stage state machines, FiFo s
- Performance, VELO appl., Subevent building, SE Buffer managemt,
- Crate Environment, Embedded / remote Control, Initialization,
- Error handling, PCI Readout, Network Interface, Eventbuilding protocols

Transport Format for Subevents



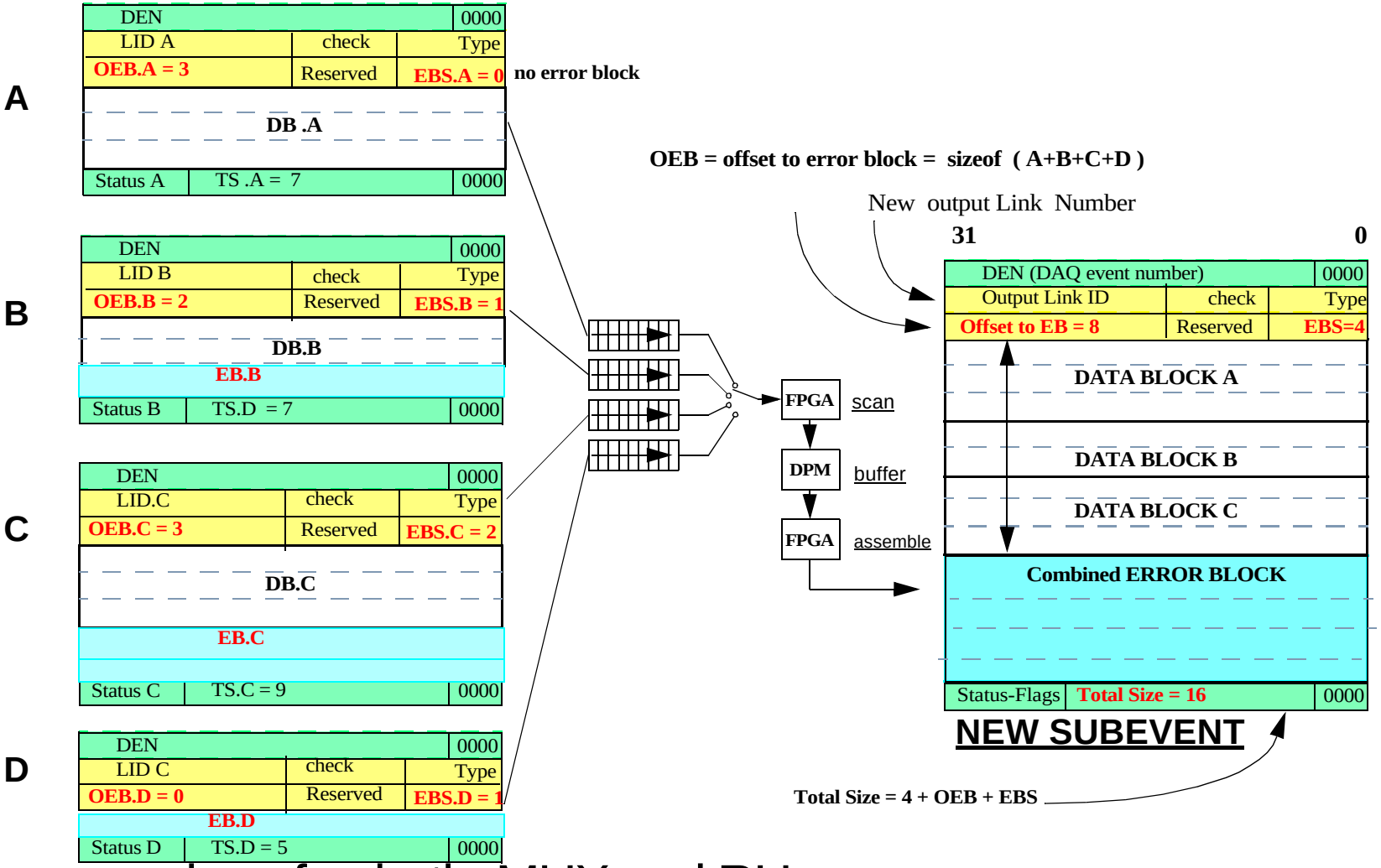
- **DAQ event identification number:** 1st level accept number, 28 bit, monotonously increasing
- **SH:** Slink 4 bit field
- **LID= Link ID**: a 16 bit field for identifying the link number to which the subevent is transmitted
- **CB= checkbits:** optional 8 bit checkbit field for the header word, default 0
- **type:** optional 8 bit field for type of data, default 0
- **OEB = offset EB:** the 32 bit offset to the optional error block in the trailor, ignored if Size EB field is zero
- **reserved:** 8 bit field, reserved (do not use until defined)
- **Size EB:** Size of error block, i.e No of 32 bit words

- **DB= Data Block:** N * 32 bit words of data (any substructures are totally transparent to the RU)
- **EB- Error Block:** Descriptors of error history of Subevent (conventions tbd.). Size miust correspond to Size EB field
- **STATUS:** 8 bits of fast status information for 8 error classes, identified by each bit, default 0
- **TS = total size (4 + EB + EBS):** 20 bit field containing total number of 32 bit words of the Subevent + header/trailor

SH/ST= Slink error status 4 bits in Header and Trailor

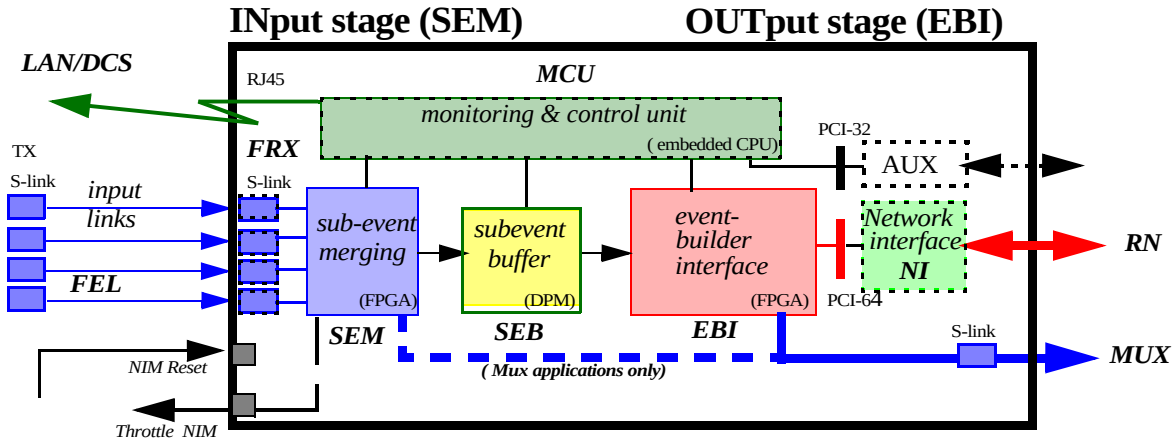
- Minimal overhead: empty SE = four 32 bit words
- Data contained is transparent to RU (independent data formats)

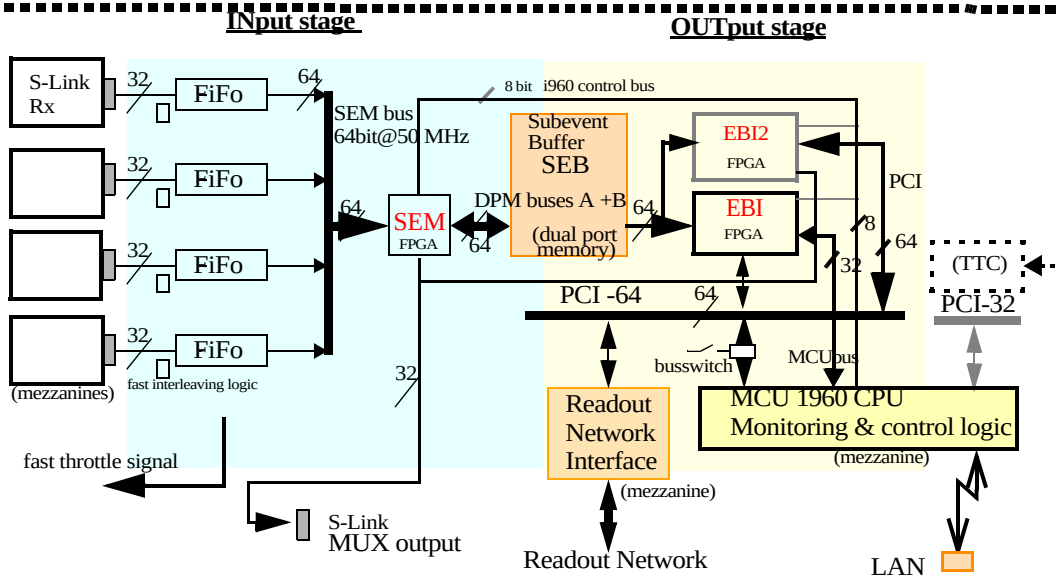
Example of Subevent Building



Same procedure for both MUX and RU

RU Architecture





Functional blocks

- SEM..... Input Merger
- SEB ..... Subev. Buffer
- EBI ..... Ev.Builder IF
- MCU ..... Mon.&Ctrl Unit
- NI ..... Network IF

Bus view

- SEM..... 64 bit -> DPM
- SEB ..... DPM 2*64 bit
- EBI ..... DPM->PCI
- MCU ..... Lan-PCI/MCU
- NI ..... RN<-> PCI

- Input state machines: SEM
- Output state machines: EBI/EBI2

Input state machines (FiFo reading)

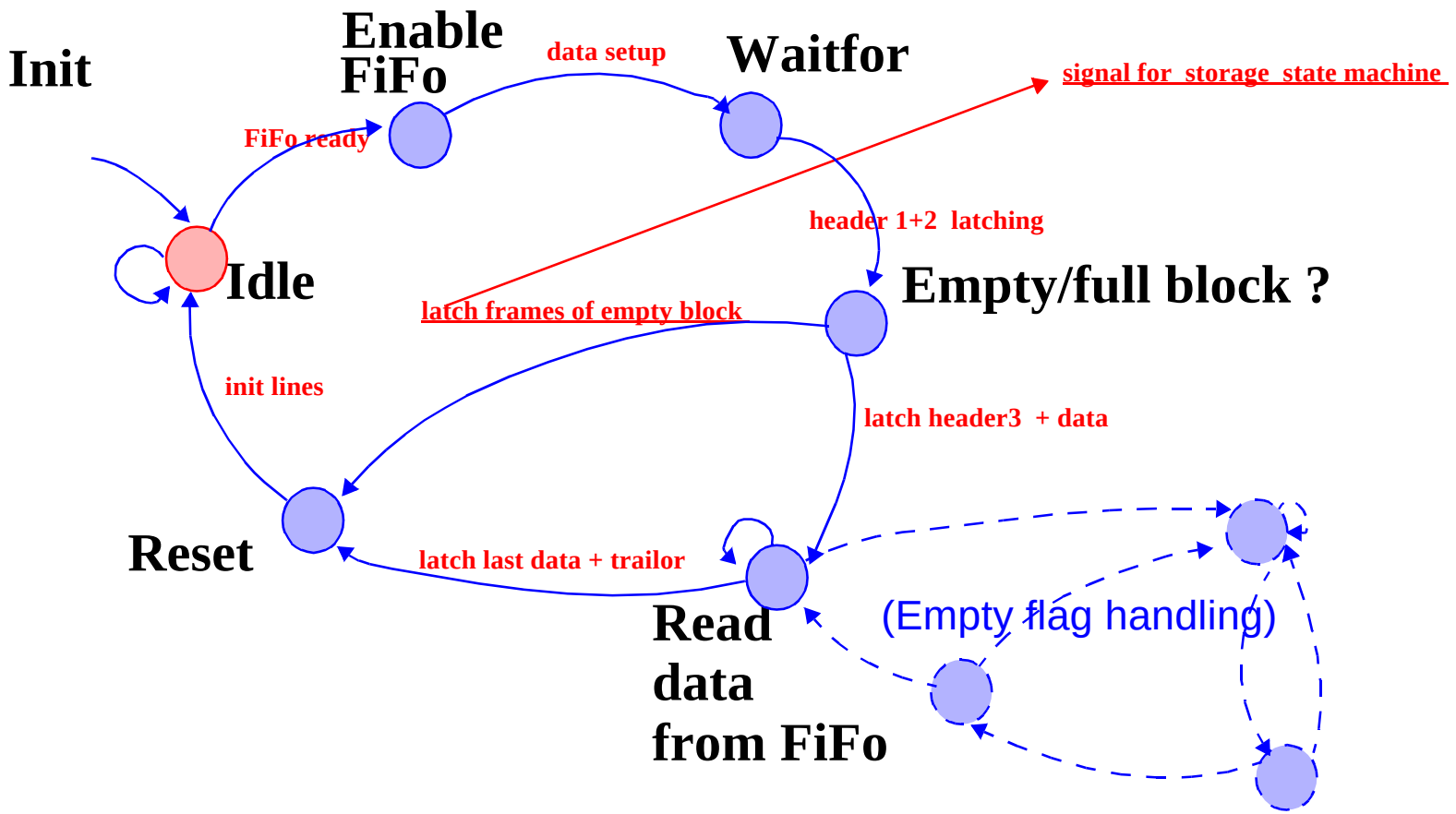
Visual HDL (D.Dominguez)

Current status:

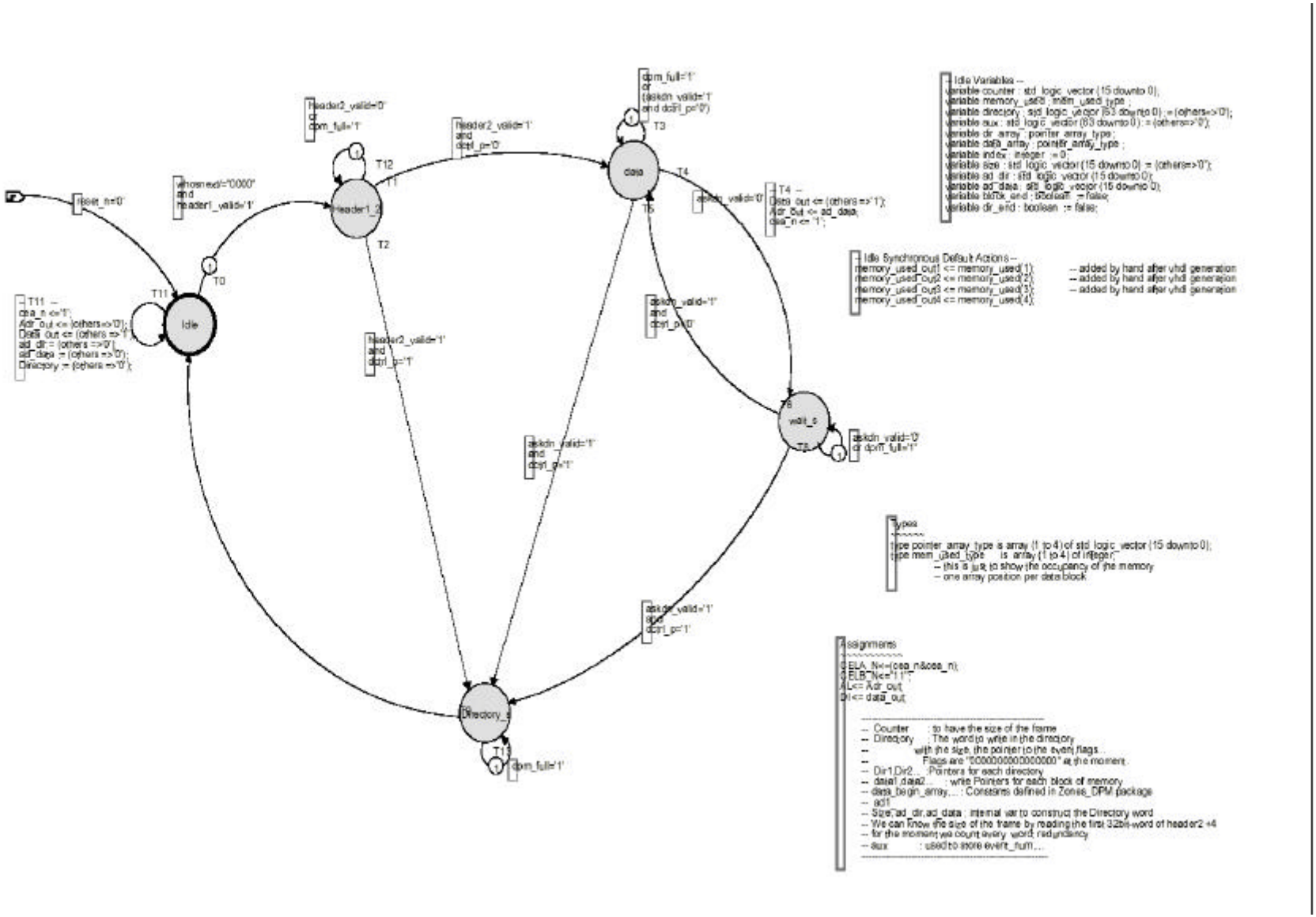
6 clocks overhead link switch

28 MHz FPGA clock (to be optimized)

State change: 1 clock



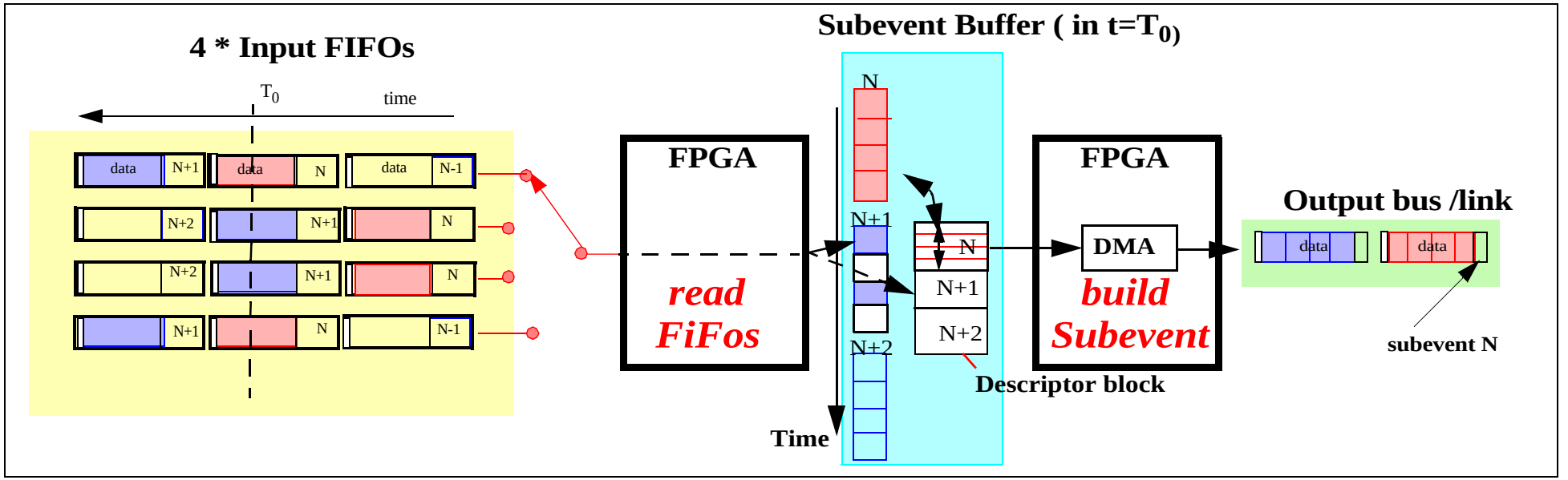
Writing to SEB -buffer



Subevent making

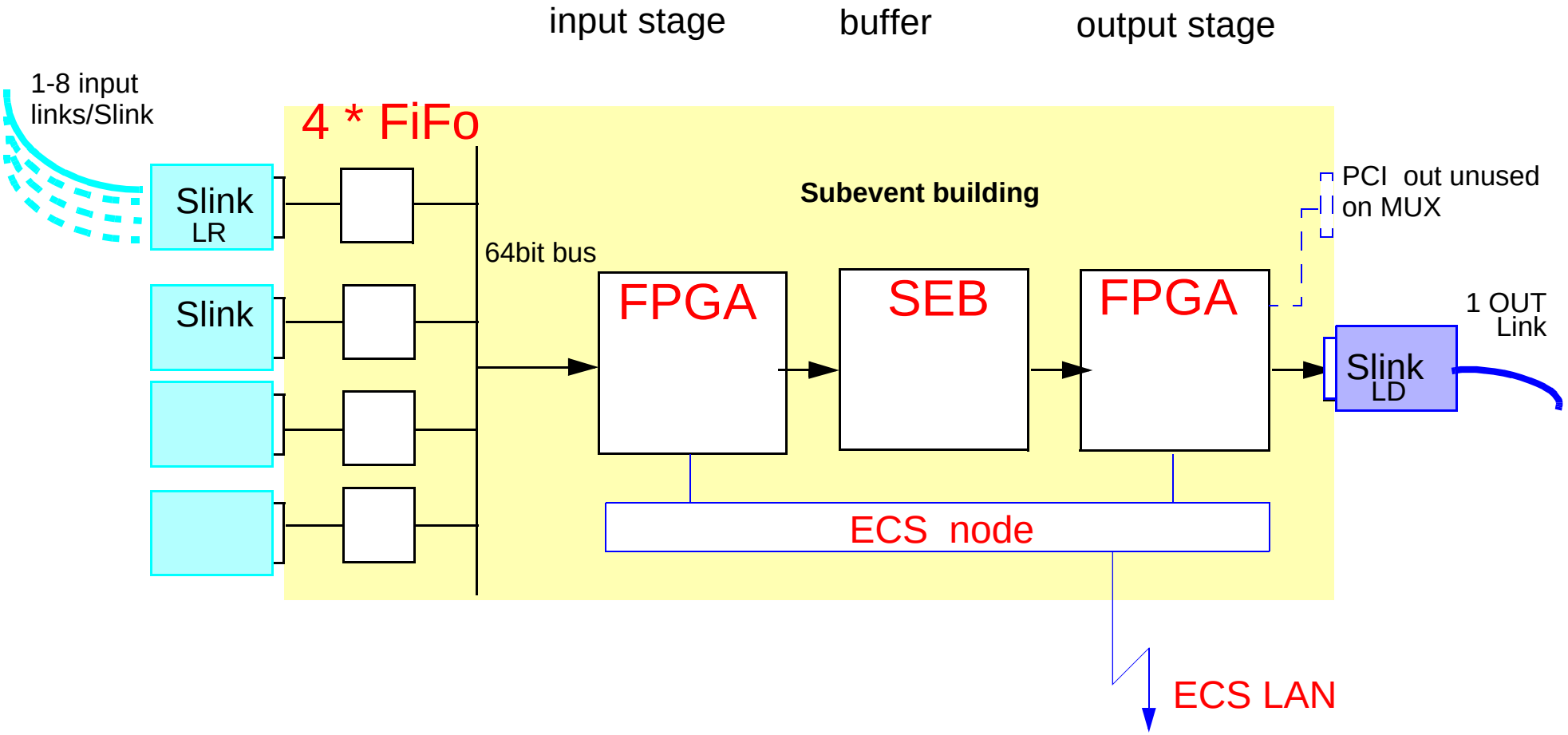
1.) read FiFos (to SEB buffer)

2.) build SEB (descriptor-DMA)*:*



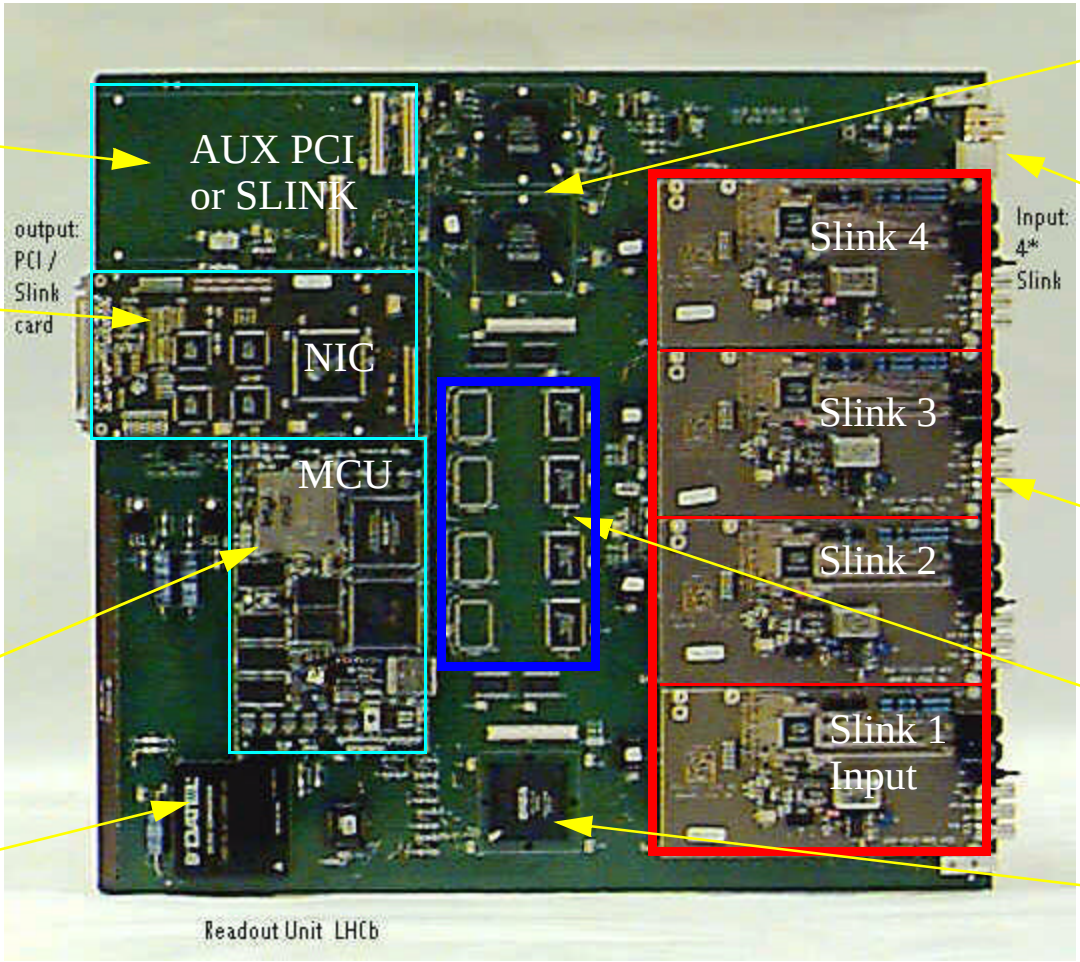
- Transport Frame: Same for input as for output
- Event-Identifiers : monotonously increasing Event Nr's used in Descriptor block for SE-building
- Timespread in arrival: compensated by buffer
- Always 1 block per input: Empty events = 4* 32 bit frame
- SE readout: descriptor based DMA always reads oldest SE from SEB
- SEB: circular buffer with overflow protection (fast throttle)

Multiplexing



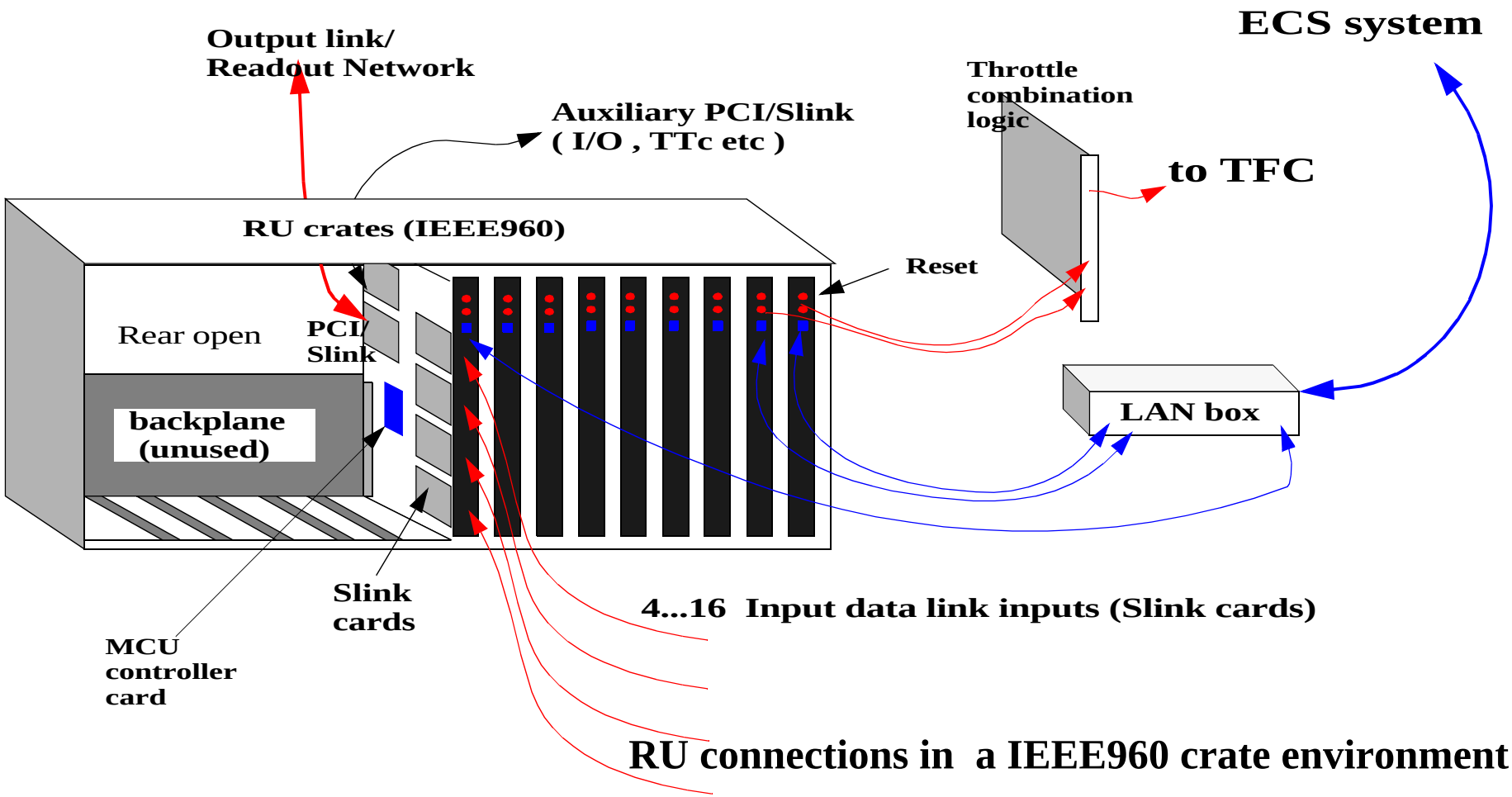
- Same as Readout Unit
- 4* Slink-in -> 1 Slink out
- up to 32 -> 1 MUX possible

RU module



- IEEE960 (9U) mechanics
- 4*Slink, 2*PMC/ Slink, 1*MCU plugin cards

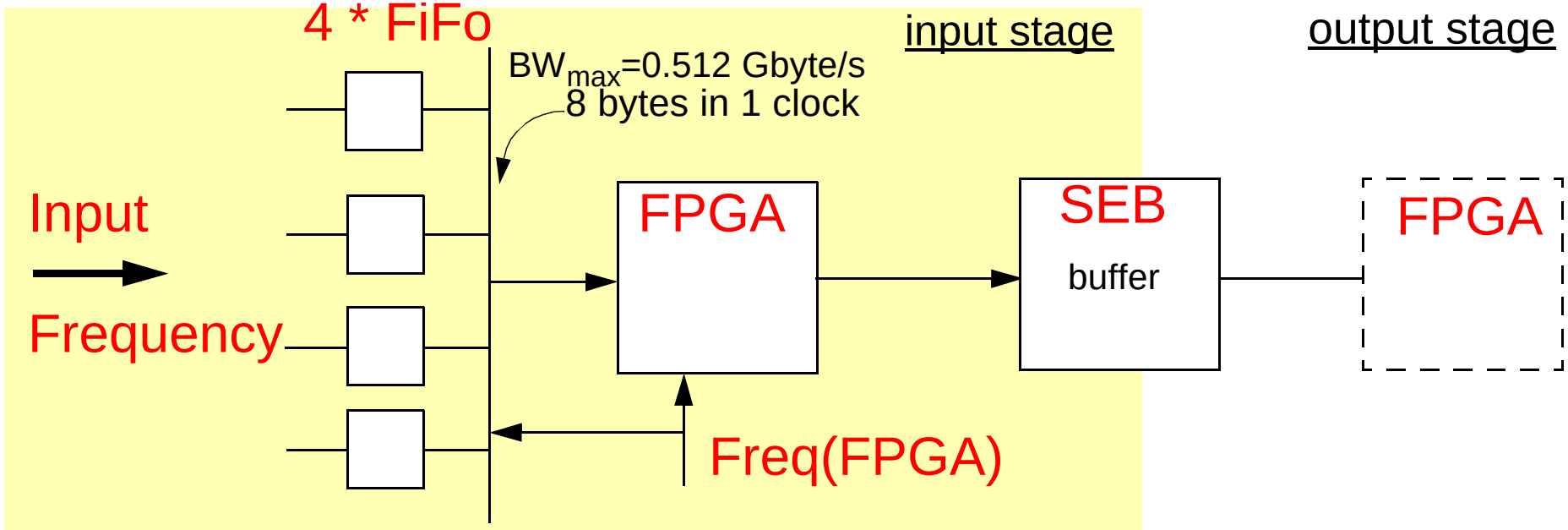
Crate environment



- Crate only for power & cooling
- Mezzanine cards for data I/O

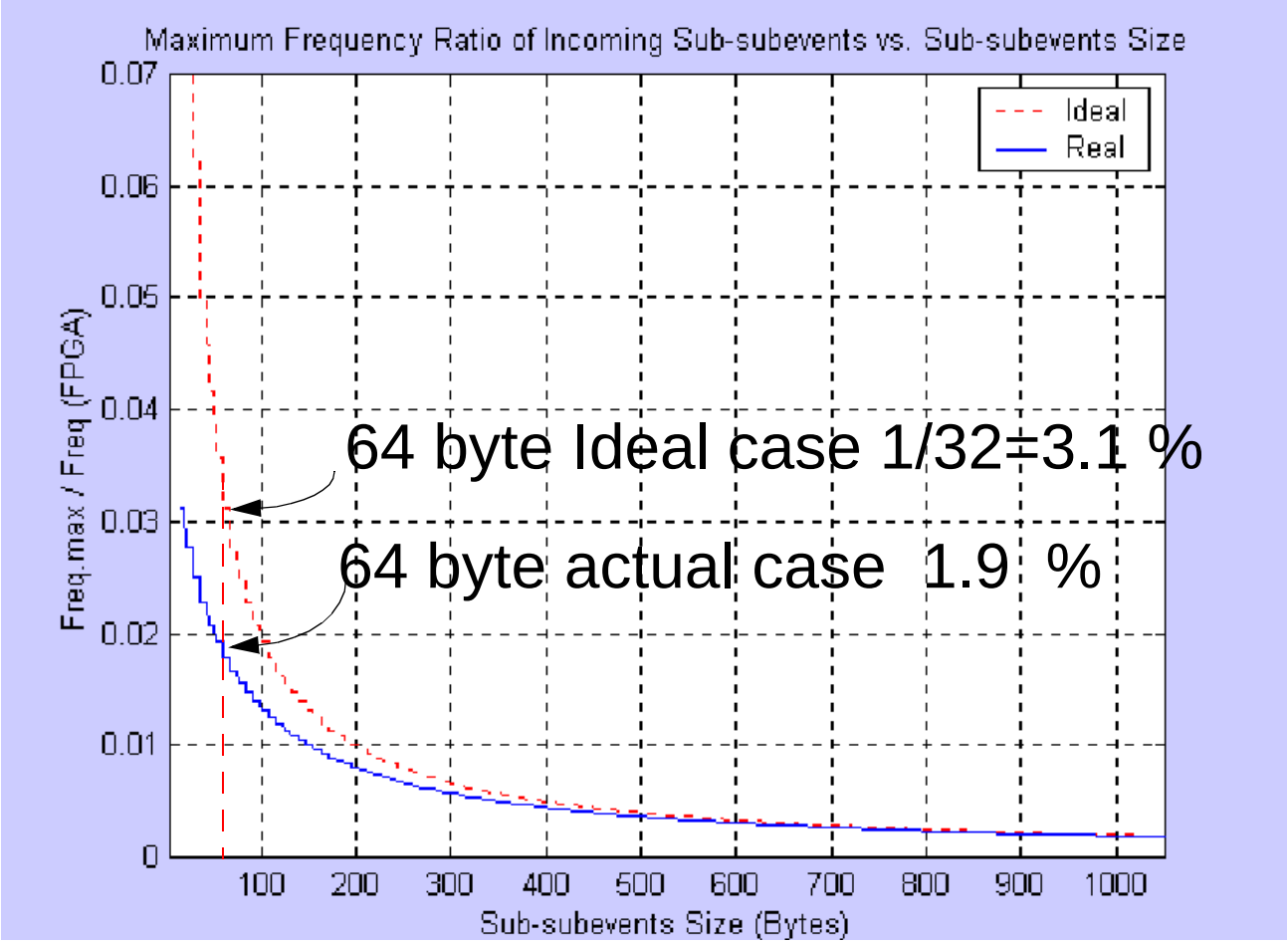
RU performance (1) Rate versus Blocksize dependencies

- Ansatz: (Frequency * blocksize) = const
  With F_{max} =1/a -> 1/ (x + a) dependency
- Theoretically: const =BW= 64byte@66 MHz = 0.512 GB/s
- Total RU erformance is product of Input stage and Output stage
- Ongoing work: input stage optimization



- Work on output stage requires understanding of DAQ protocols
- Work on output stage (PCI) started for VELO

RU Performance (2) 1/(a+x) in real



Ratio of FPGA clocking rate over input rate in

a.) ideal case : 3.1%

64 byte require 8 clocks and 4 inputs -> Input rate is 32 less than FPGA clock

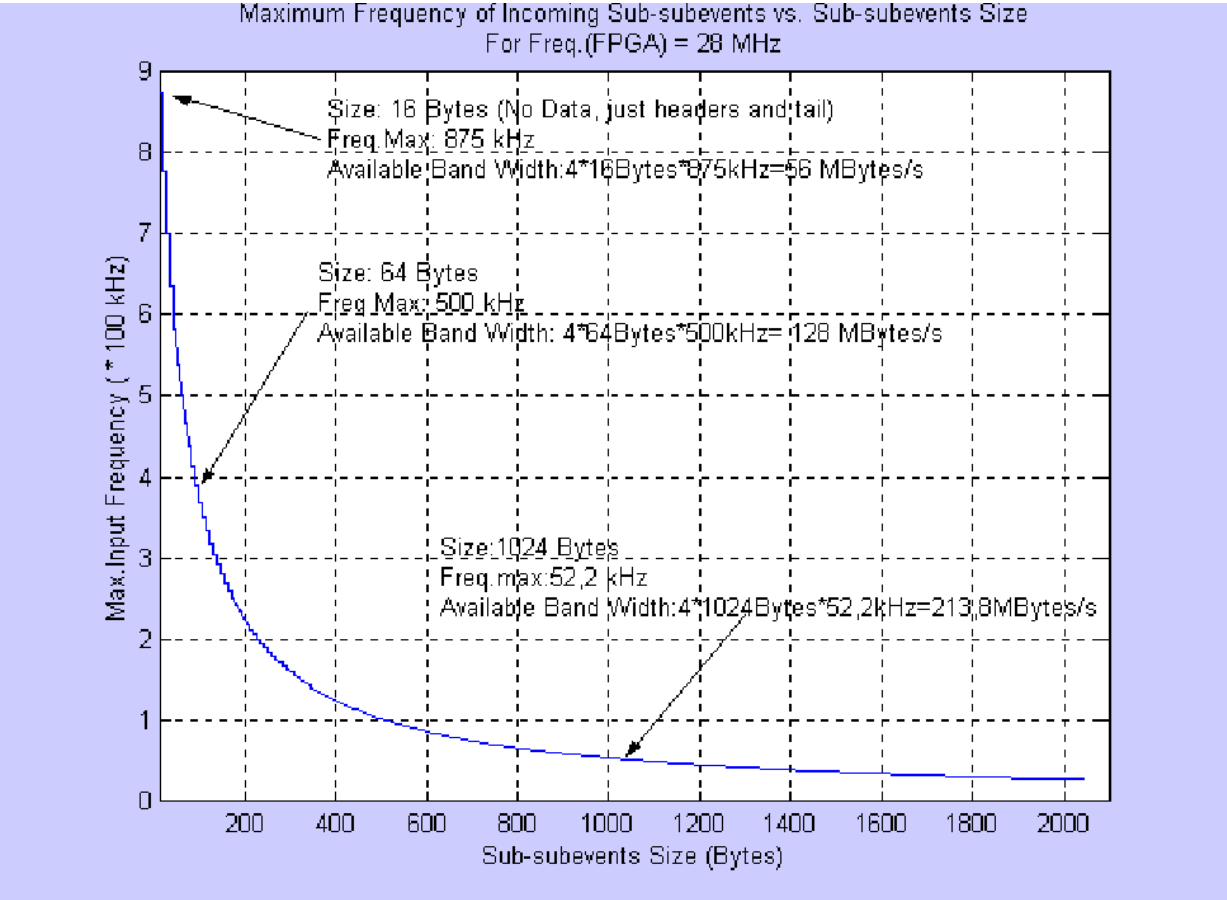
b.) actual case

Switching overhead between link inputs (6 clk)

- 6 clock link switching overhead critical for short blocks (VELO)
- DAQ operation (>200 byte) not critical

RU performance (3) Actual situation (being tuned)

- 28 MHz state machine
- 6 clock switching between links



Current state machine:

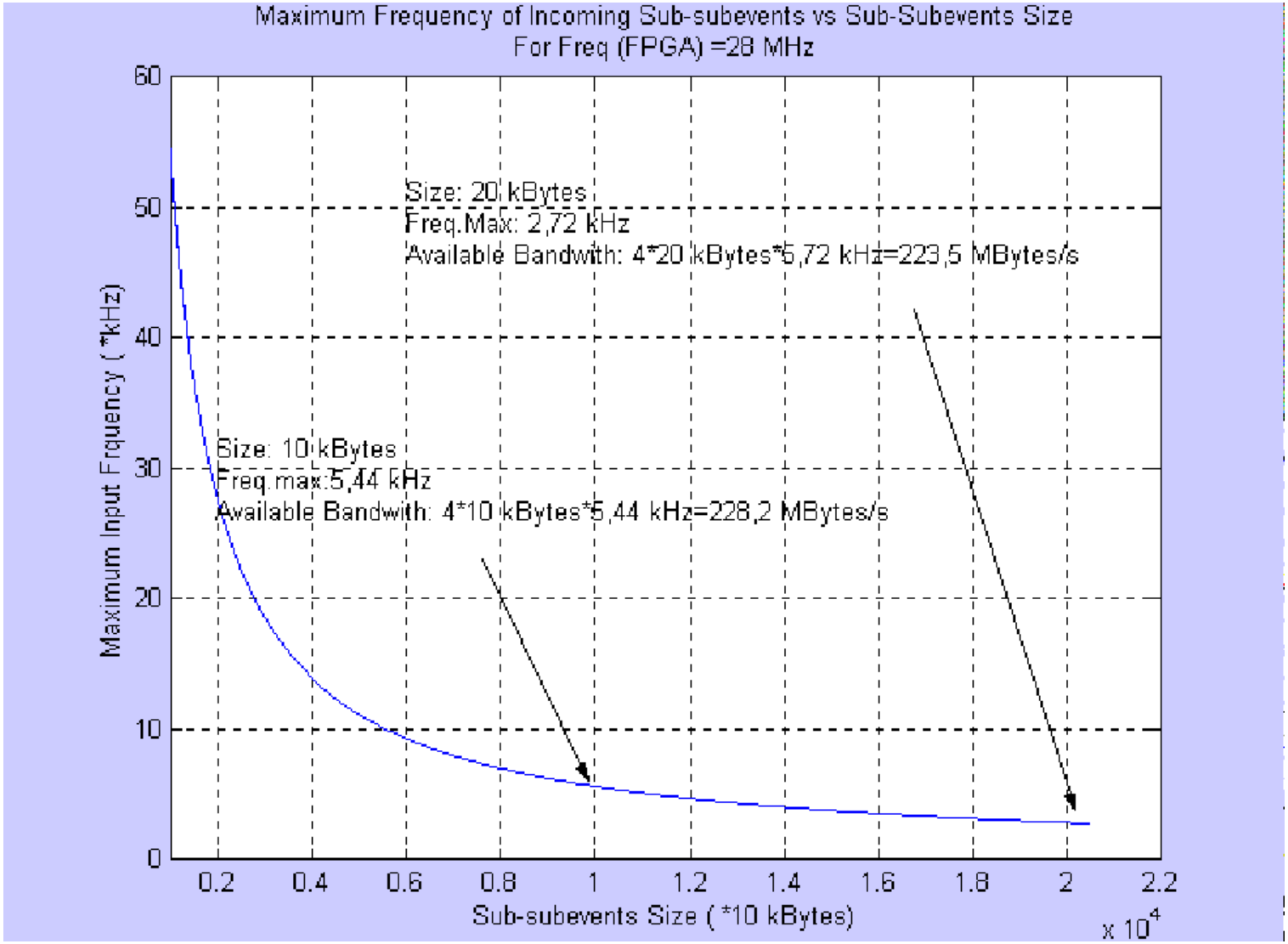
- DAQ 1 kB @ 52.2 kHz
- VELO* 64byte@0.5MHz

* Factor two in product

$Freq_{FPFA}$ * clock-overhead

required for VELO operation

RU Performance (4) Long events

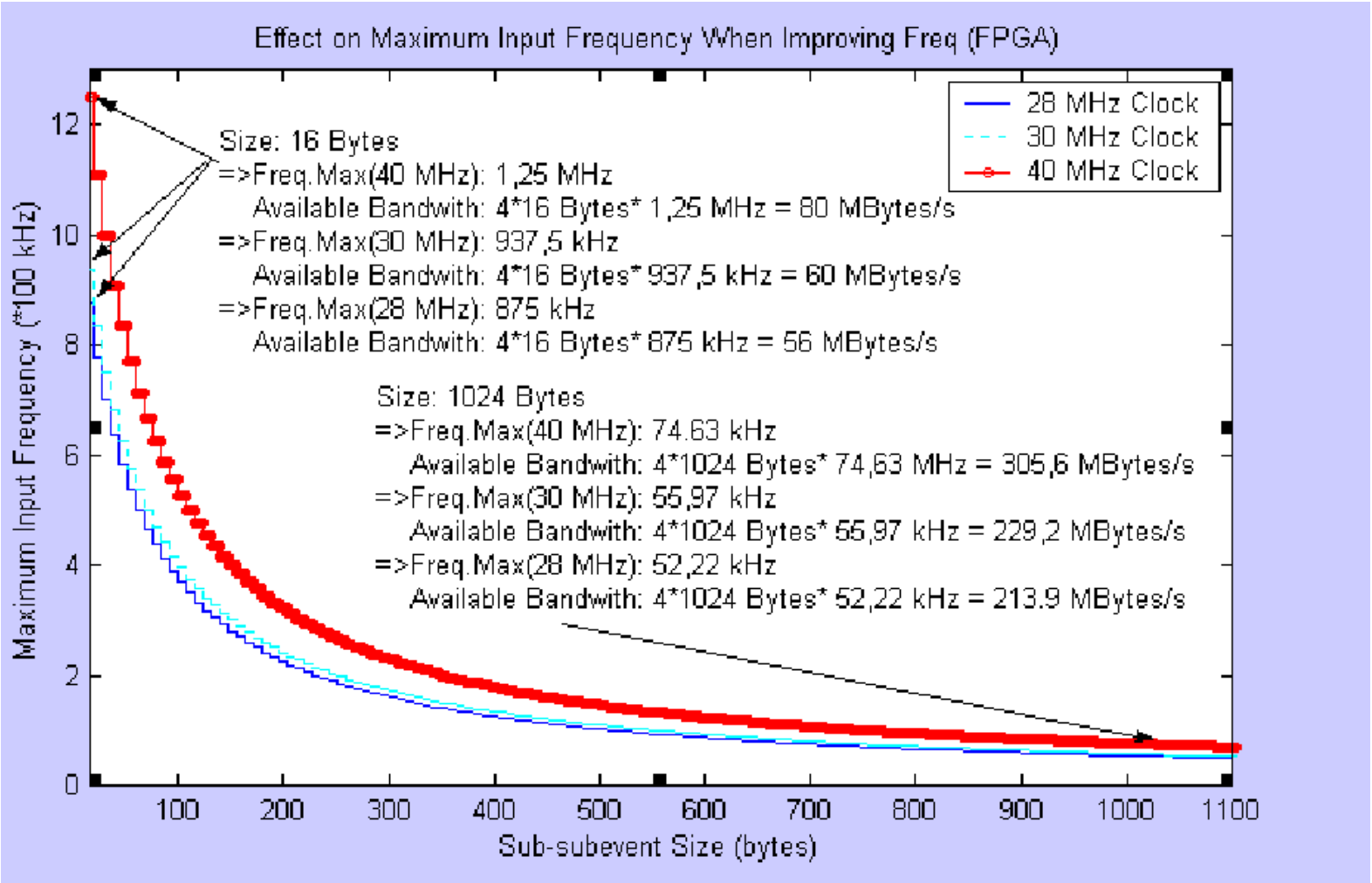


Non-zero sup-pressed data:

10 KByte @ 5.4 kHz

20 kByte @ 2.72 kHz

RU performance (5) Possible Improvements (F_{fpga})

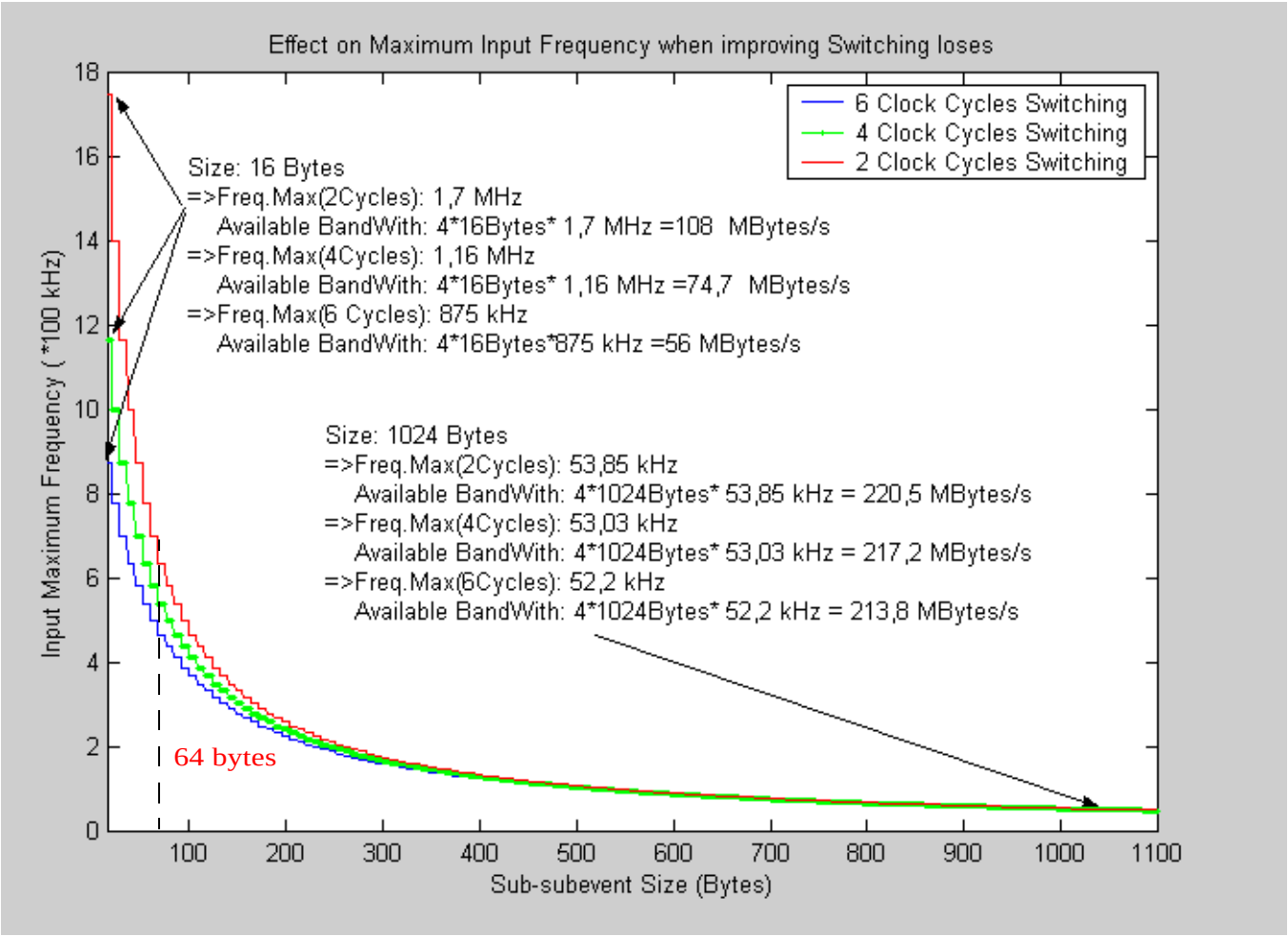


State machine clocking -> up to 66 MHz theoretically

Mainly interesting for short blocks

VELO: required clocking > 40 MHz

RU Performance (6) Possible improvement (Switching)



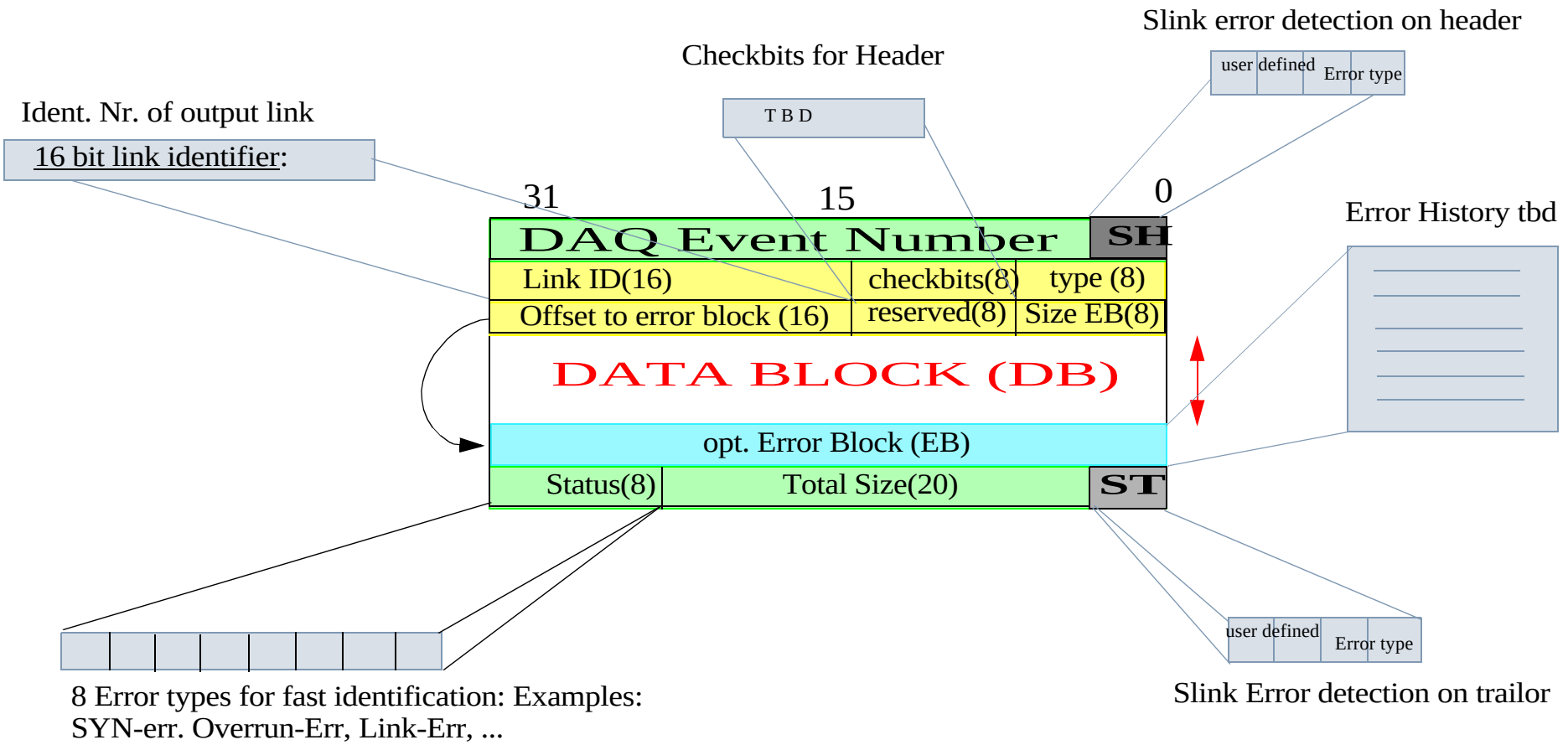
Main improvement required for VELO 64 bytes operation:

Clock overhead reduction for link switching

from 6 > 4 clocks gains ~ 30% in input rate

Improvement: deserialisation of state machines

Error handling



- Error tagging : fast, 8 different bits
- error types and handling .. tbd
- Error rate monitoring per type possibl
- Clear function for bulk error streams ?
- Error history block entries... tbd
- Header protection ...optional

Status

- 2 Protos in use, 2 more being prepared.
- 4 LHCb pattern generators (Slink card F.Bal) in use
- No major problems detected so far, FPGA performance tuning.
- Work on output stage (Subevent transmission, PCI initialization, NIC adressing) started
- Revision list for revision RU module being compiled
- Applications: DAQ, MUX, VELO

- How to get involved: RU meetings Wednesdays 161-r-009 9:00
- Docs/Status: http://www.cern.ch/~hmuller/readout_unit.htm
- RU distribution/discussion readoutunit@lhcb.cern.ch